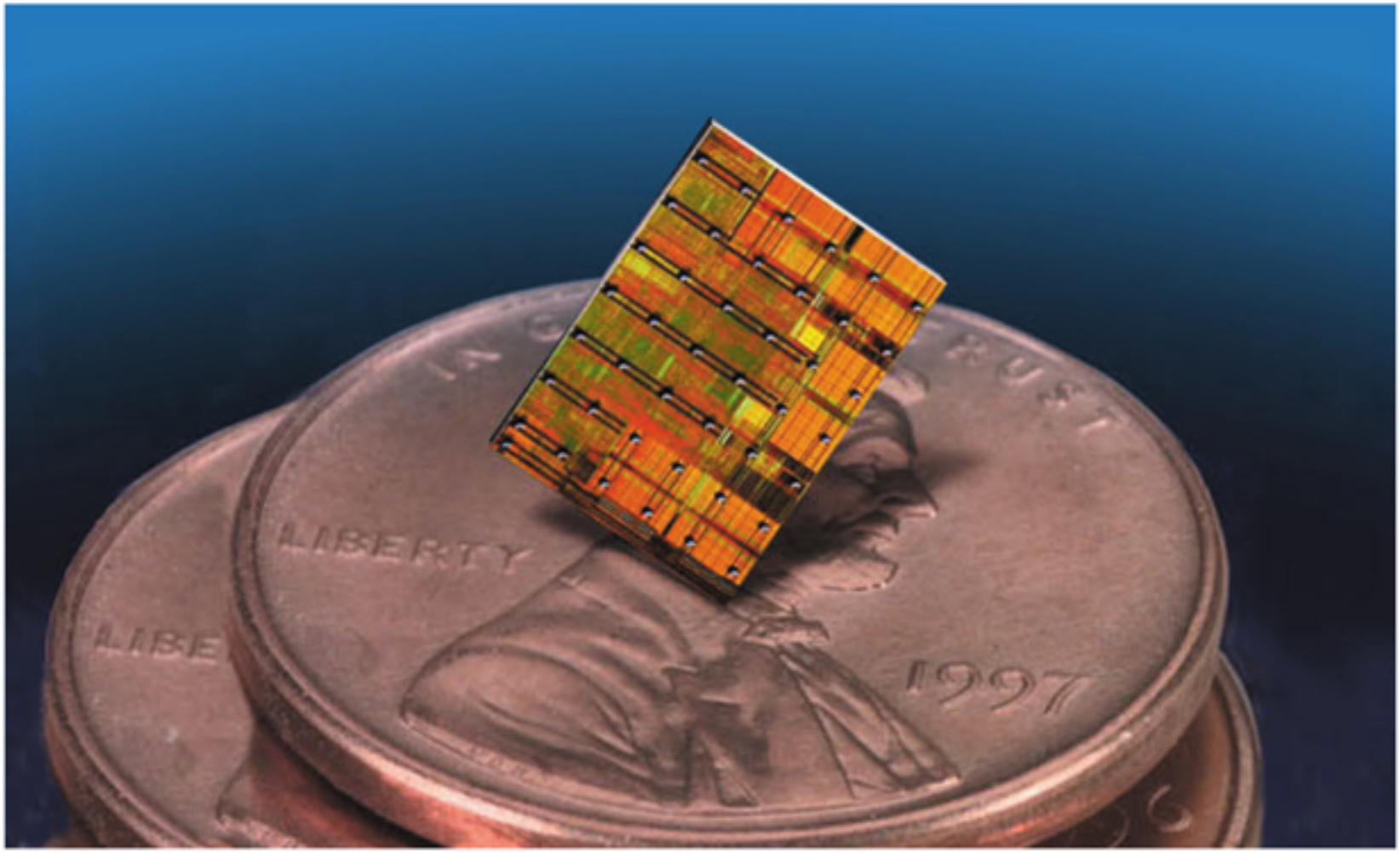
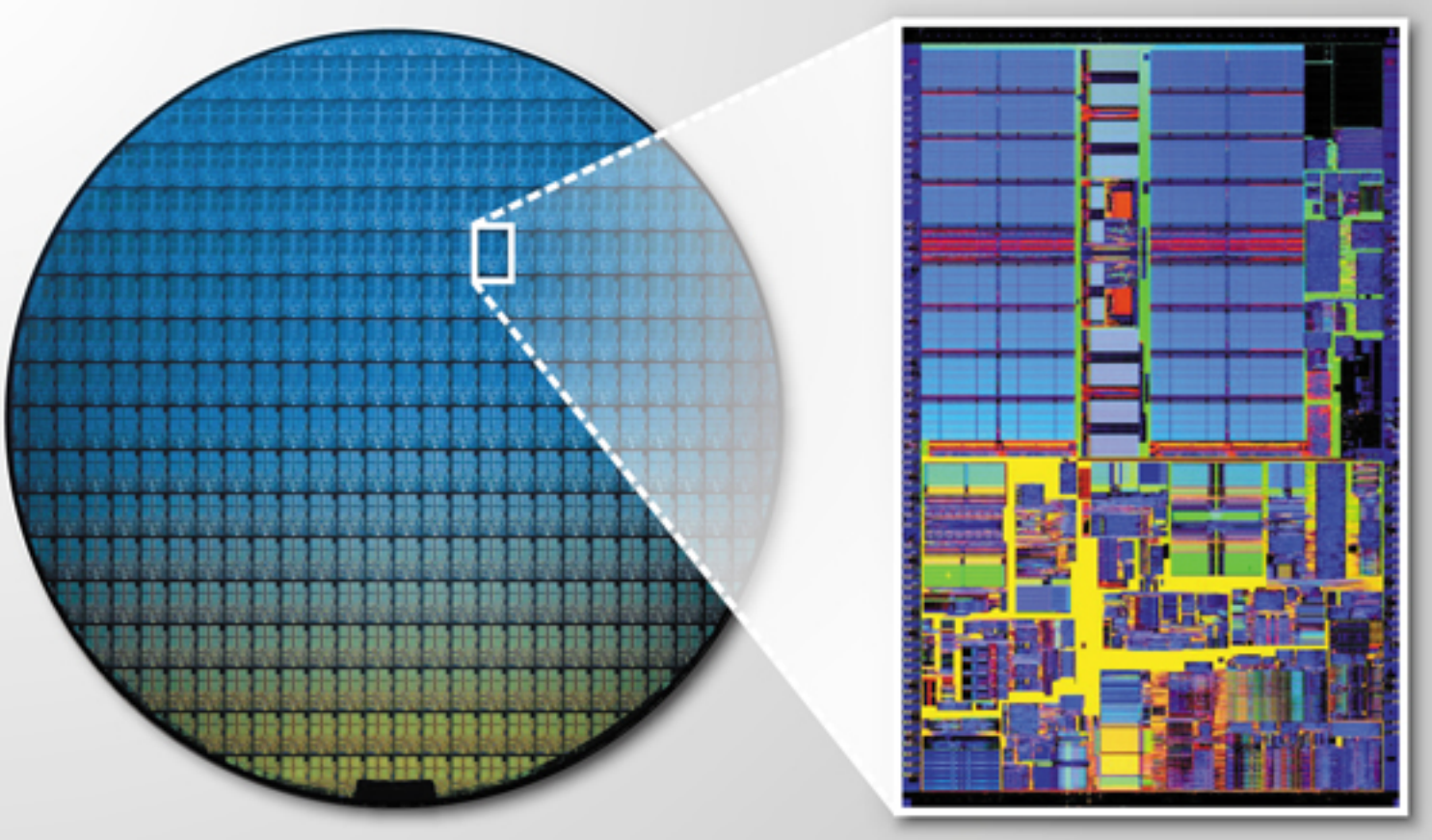
Current Applications of Integrated Circuits ("Chips")

Today, Chips Must Contain Millions of Components, Yet Be Very Small in Size



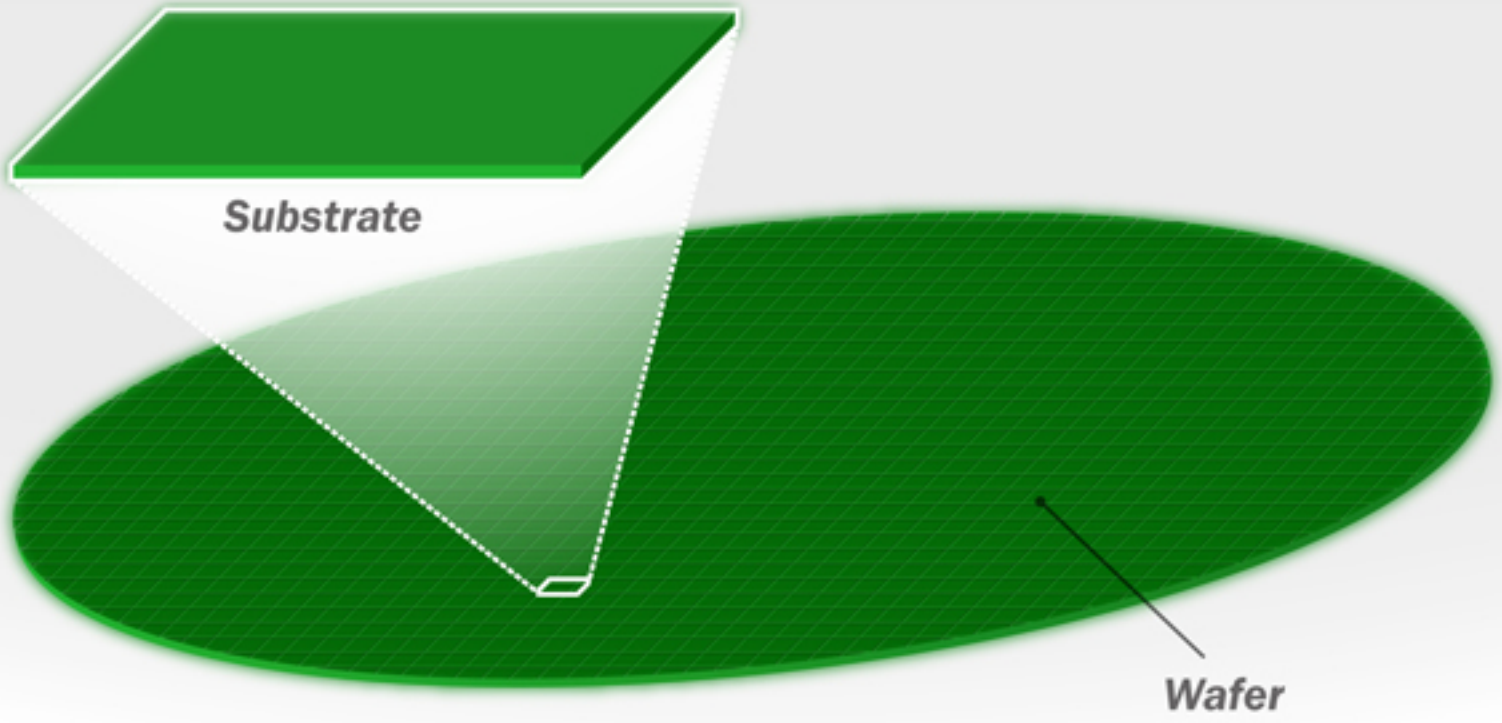
Each Silicon Wafer Is Capable of Yielding Hundreds of Individual Chips



Source: www.sandpile.org/impl/pics/intel/p3/wafer_13.jpg

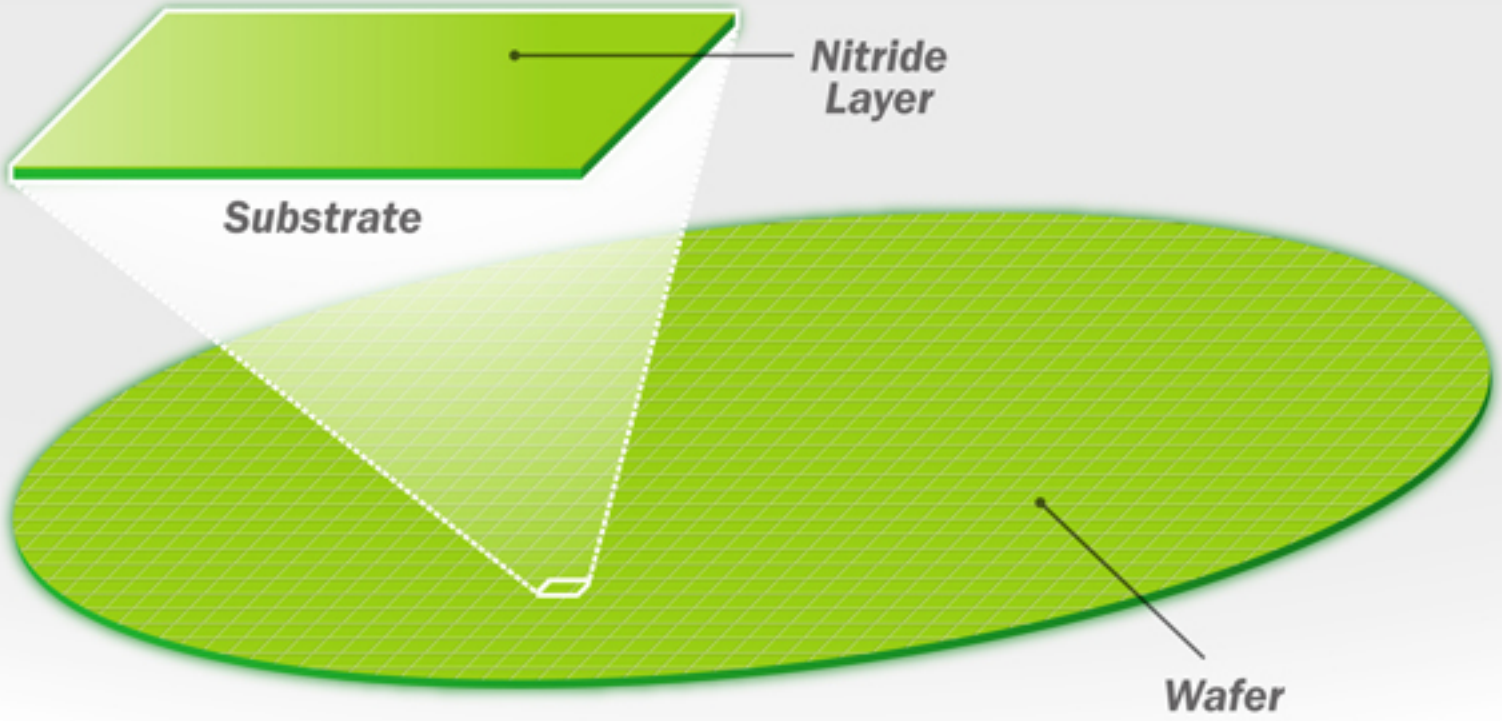
Semiconductor Wafer at the Beginning of a Typical STI Process

PRIOR ART



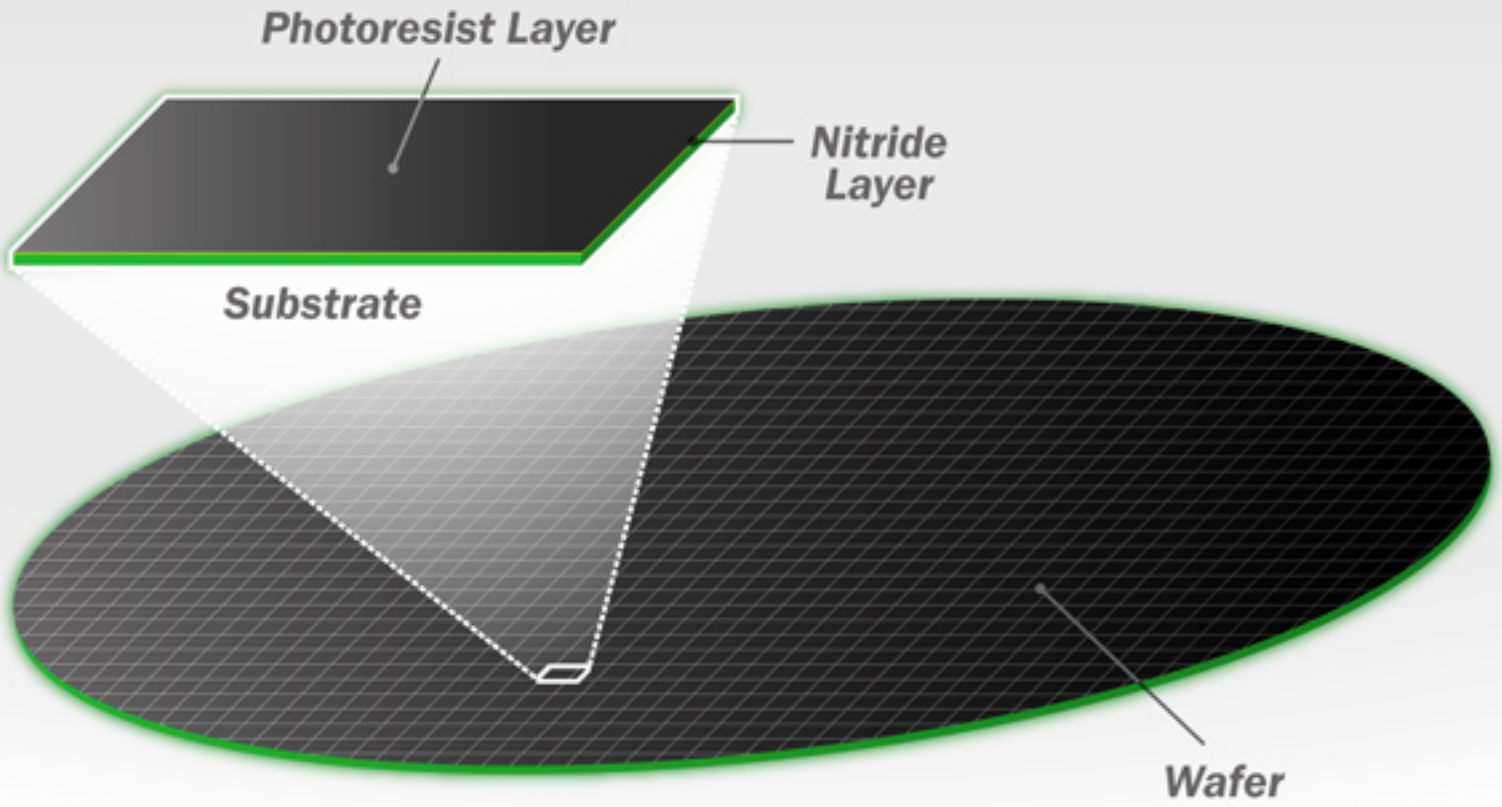
Nitride Is Deposited on Substrate

PRIOR ART



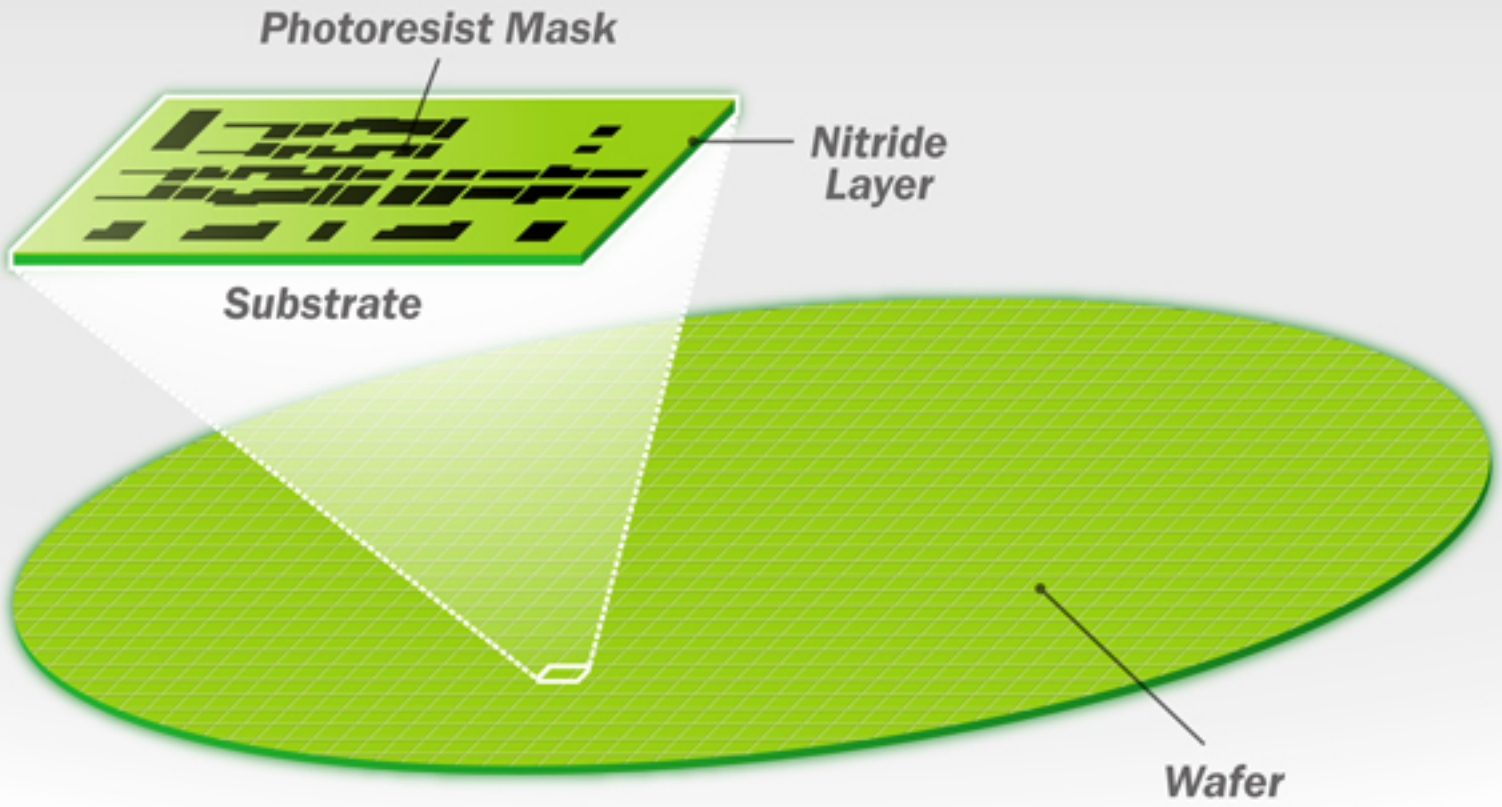
Photoresist Is Deposited on Top of the Nitride Layer

PRIOR ART

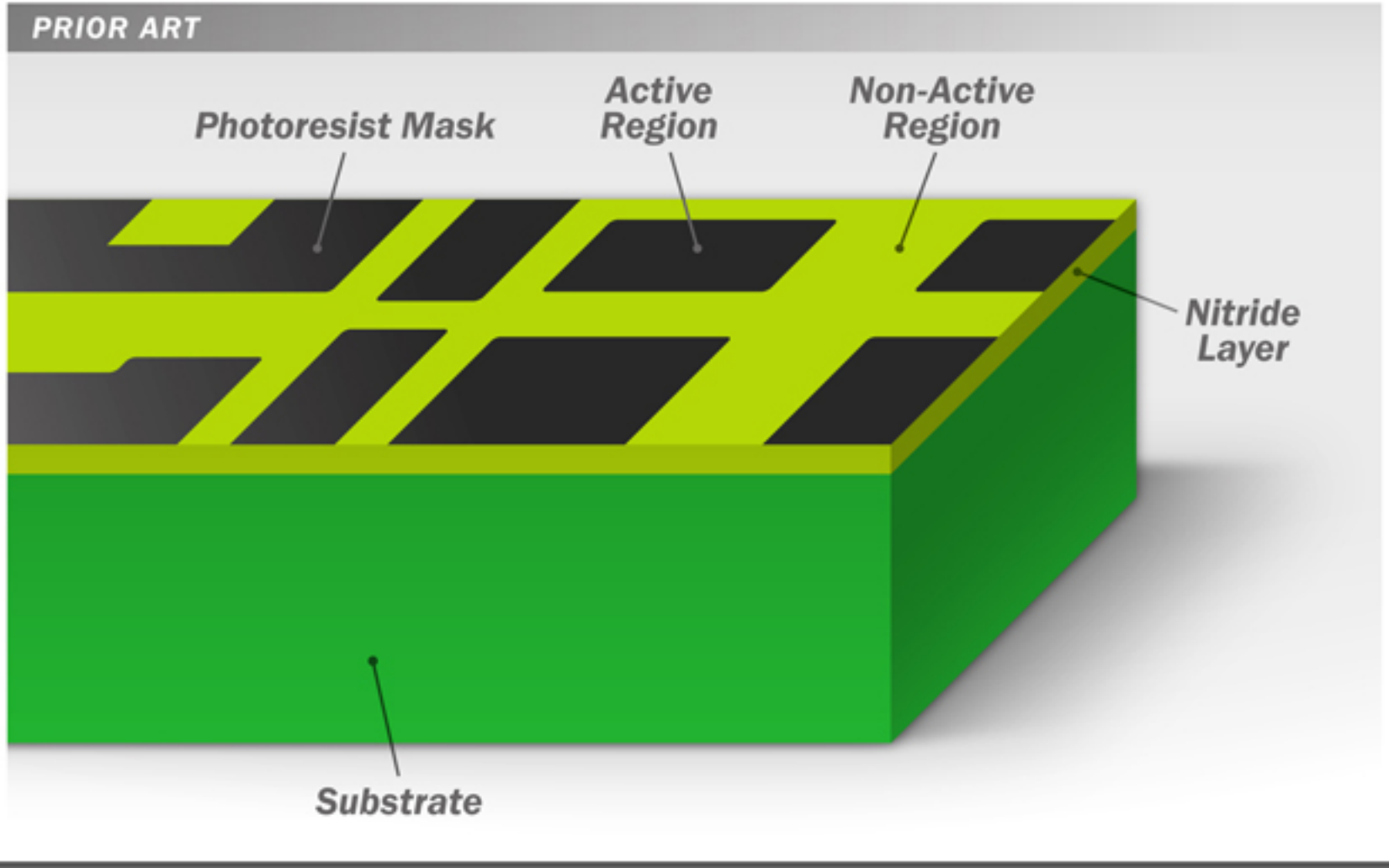


Photoresist Not Covered by a Mask Dissolves, Exposing the Nitride Layer Underneath

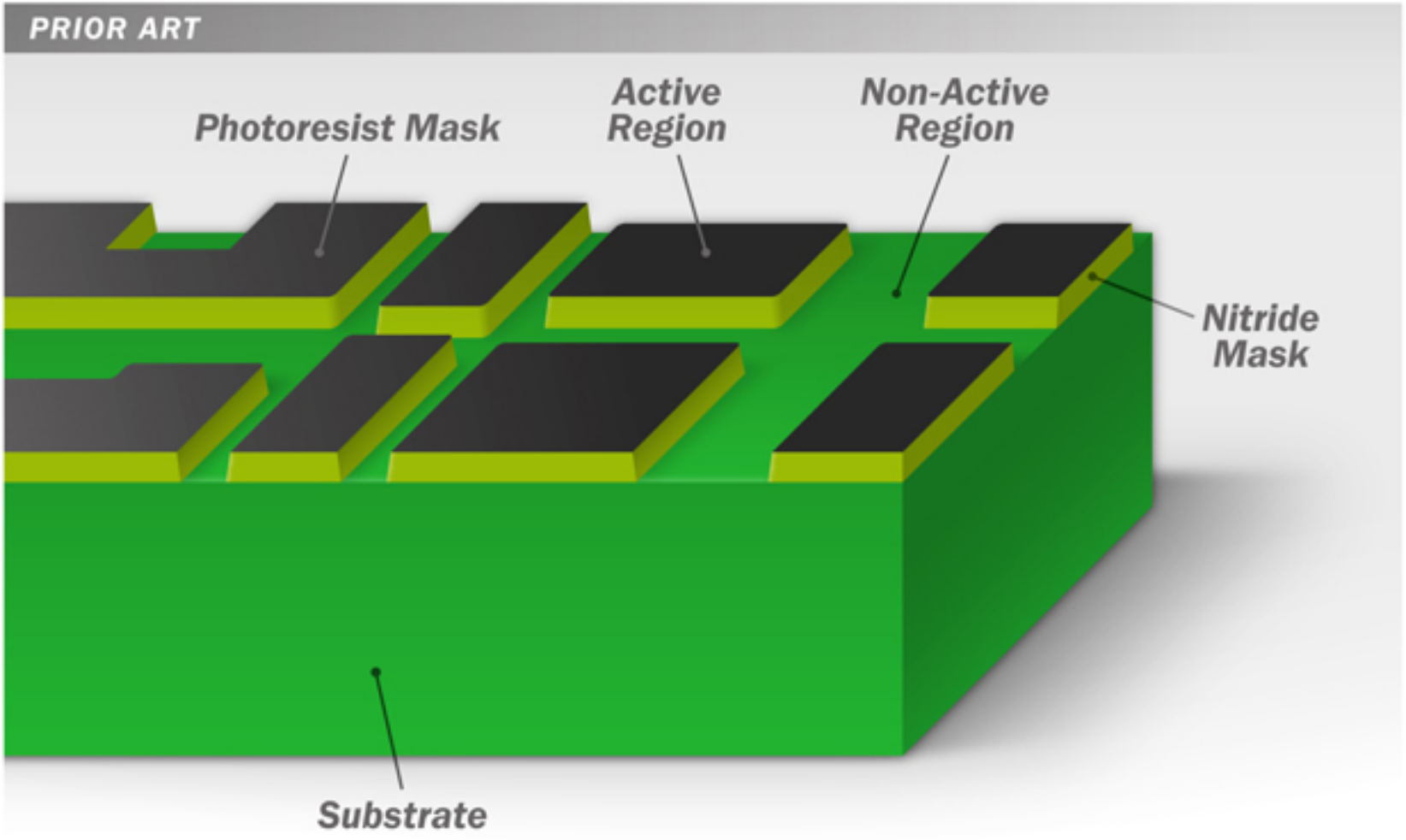
PRIOR ART



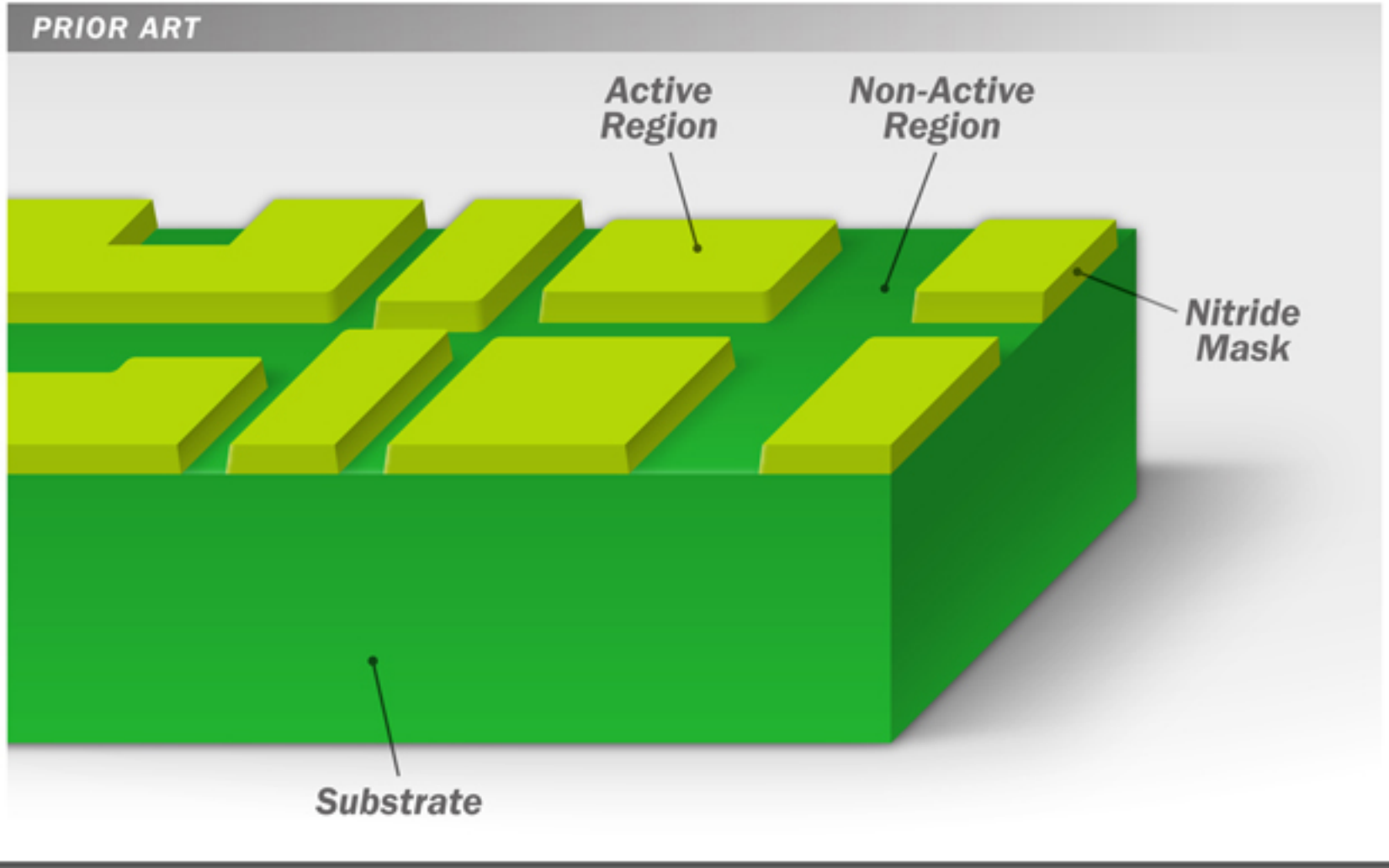
The Photoresist Mask Defines the Locations of Active Regions



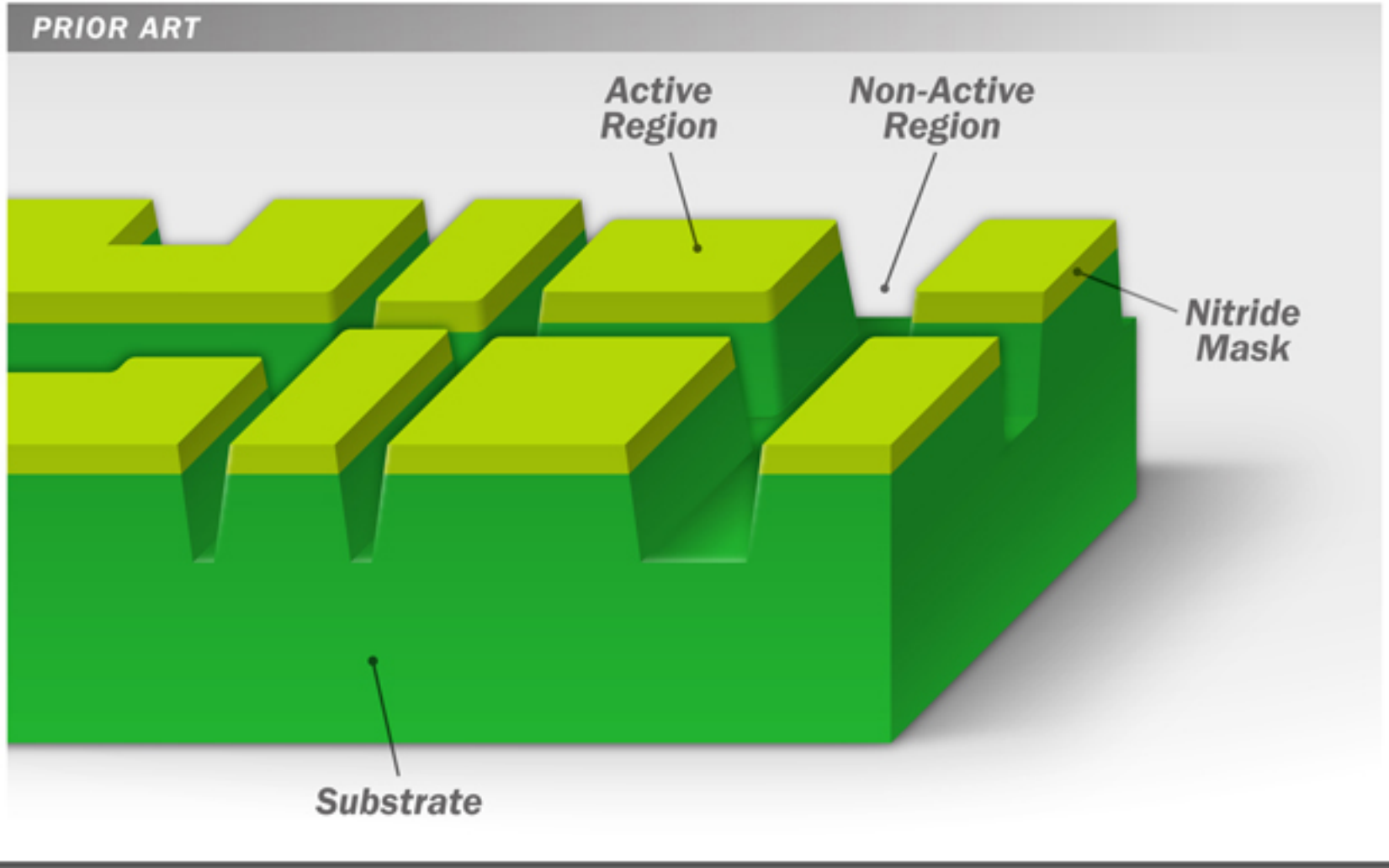
The Exposed Nitride in the Non-Active Regions Is Removed



The Remaining Nitride Layer Masks the Active Regions



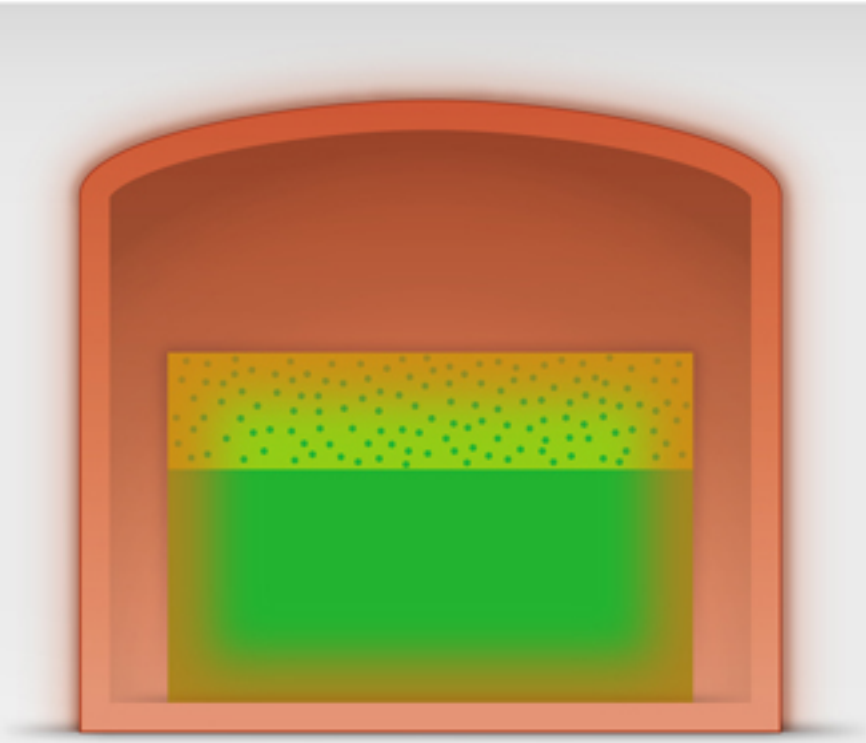
Trenches Are Etched into the Exposed Non-Active Regions of the Substrate

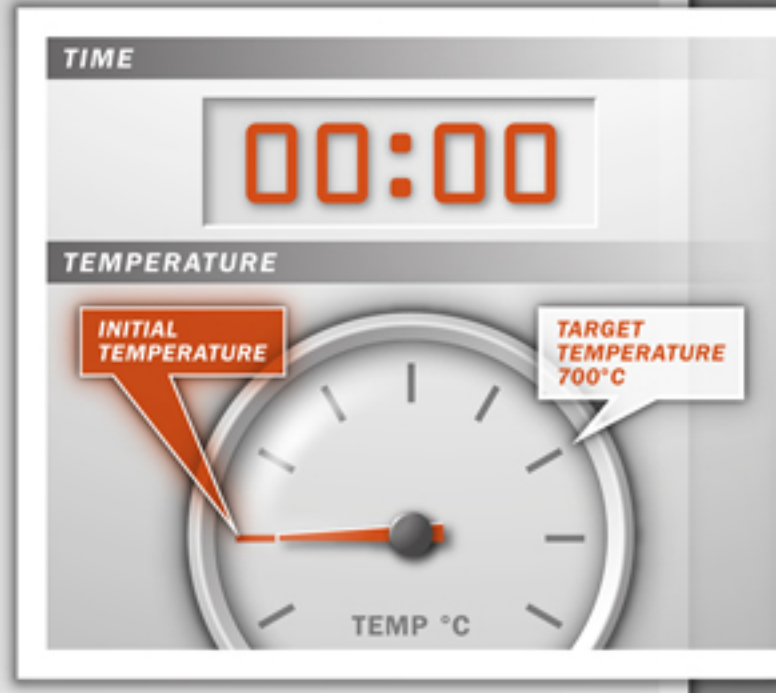


Method for Manufacturing a Polycrystalline Layer on a Substrate

An amorphous silicon layer is deposited.

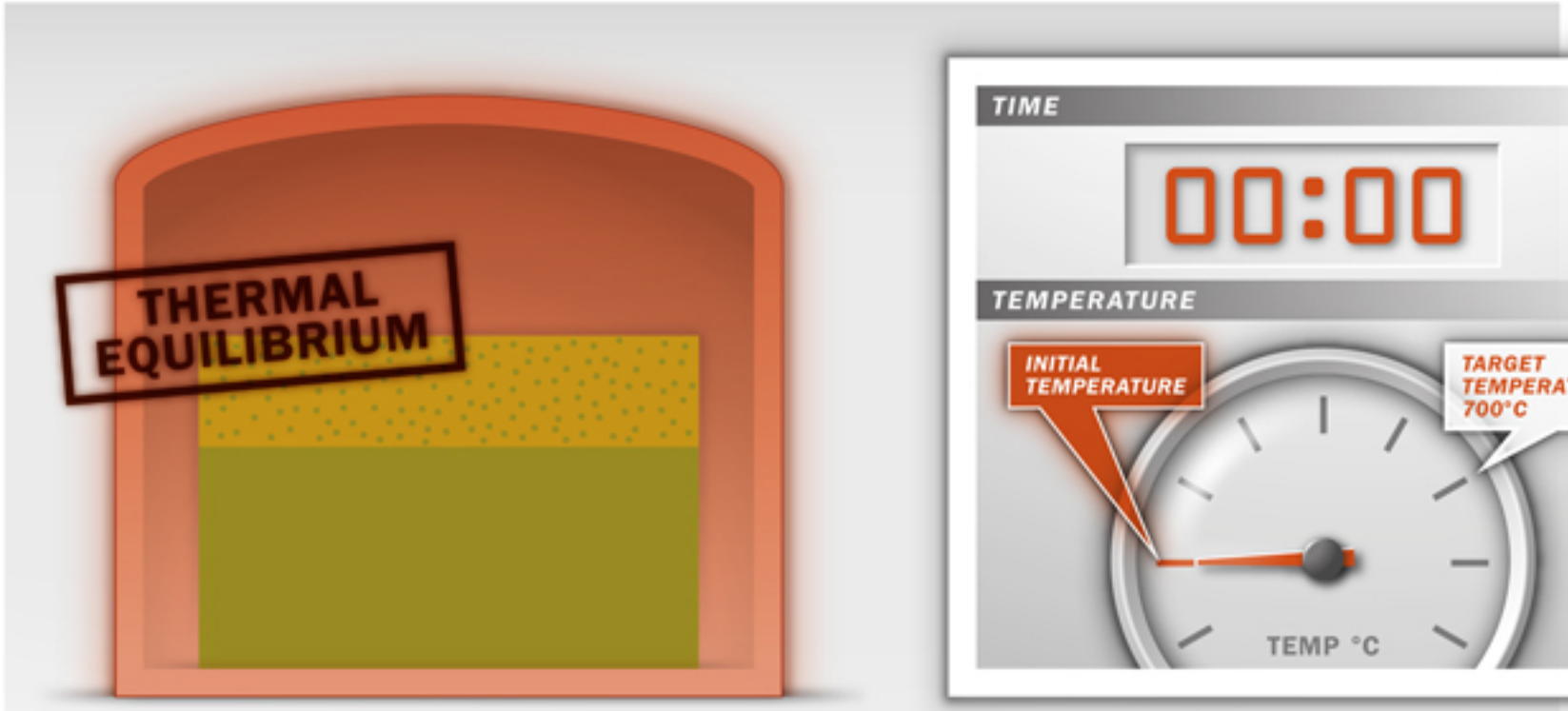
Method for Manufacturing a Polycrystalline Layer on a Substrate





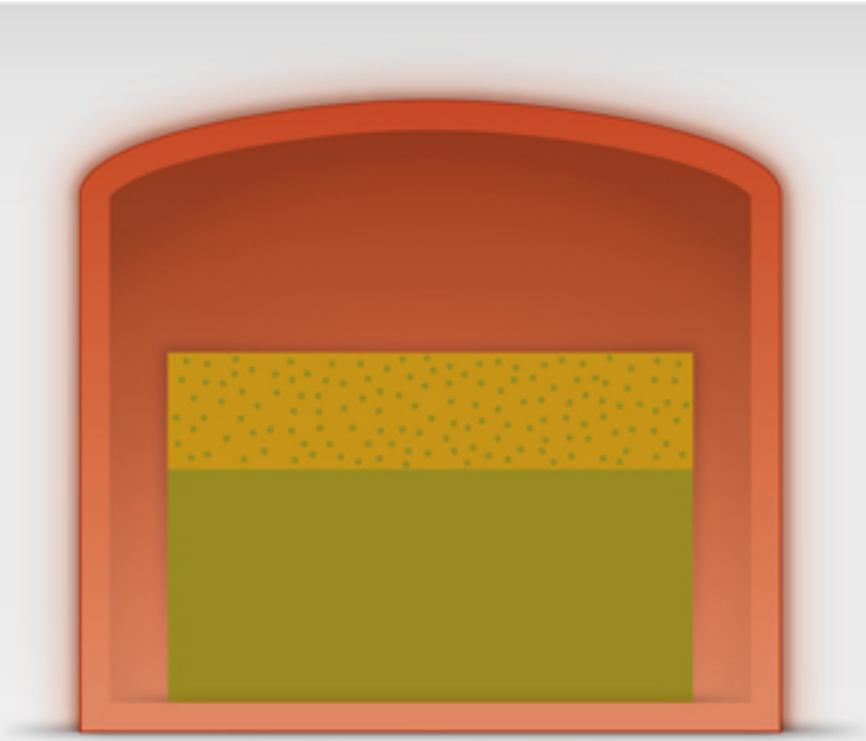
Substrate with amorphous layer is heated to an initial temperature that is LOWER than the crystallization temperature.

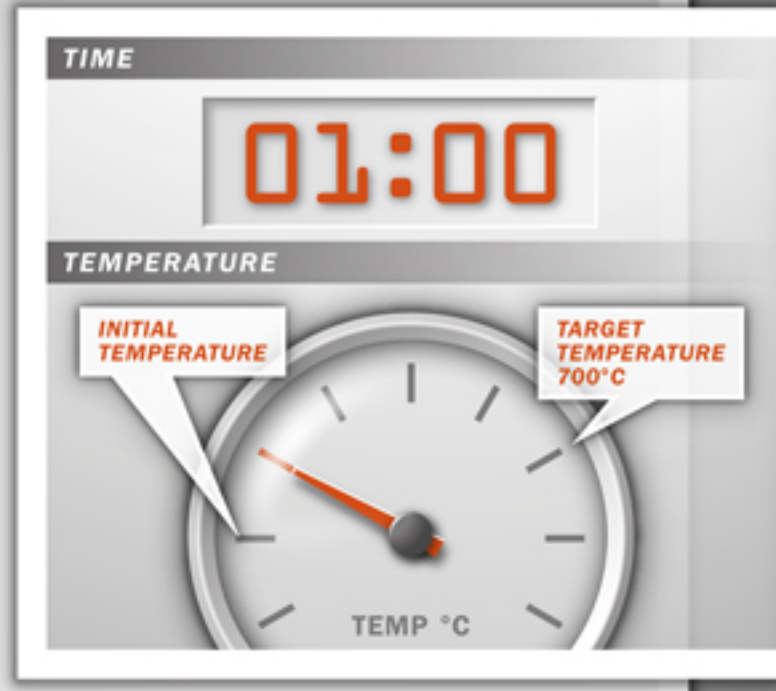
Method for Manufacturing a Polycrystalline Layer on a Substrate



Substrate with amorphous silicon layer is held at initial temperature to achieve a thermal equilibrium.

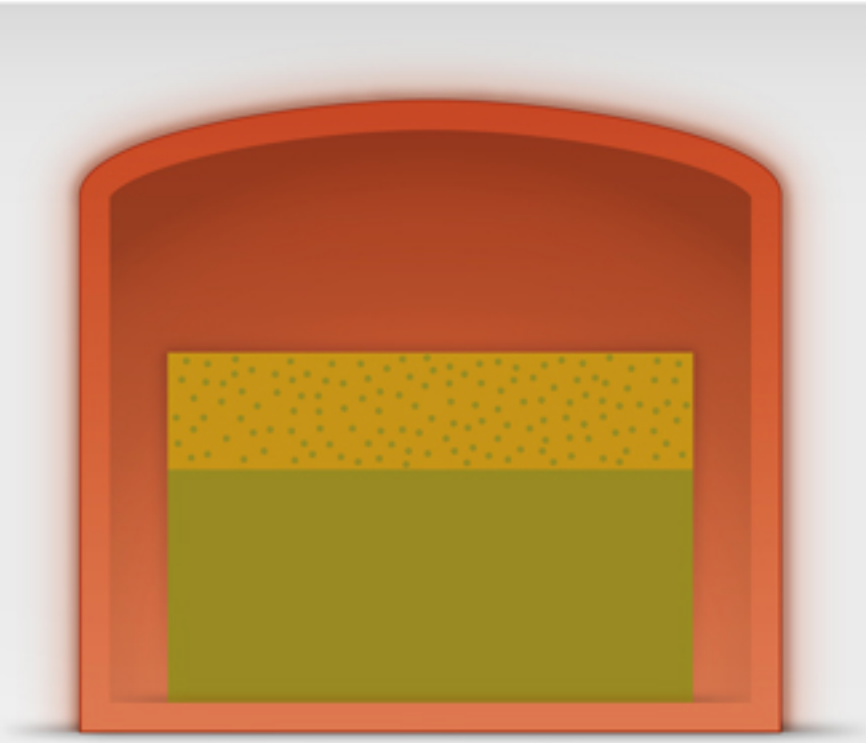
Method for Manufacturing a Polycrystalline Layer on a Substrate

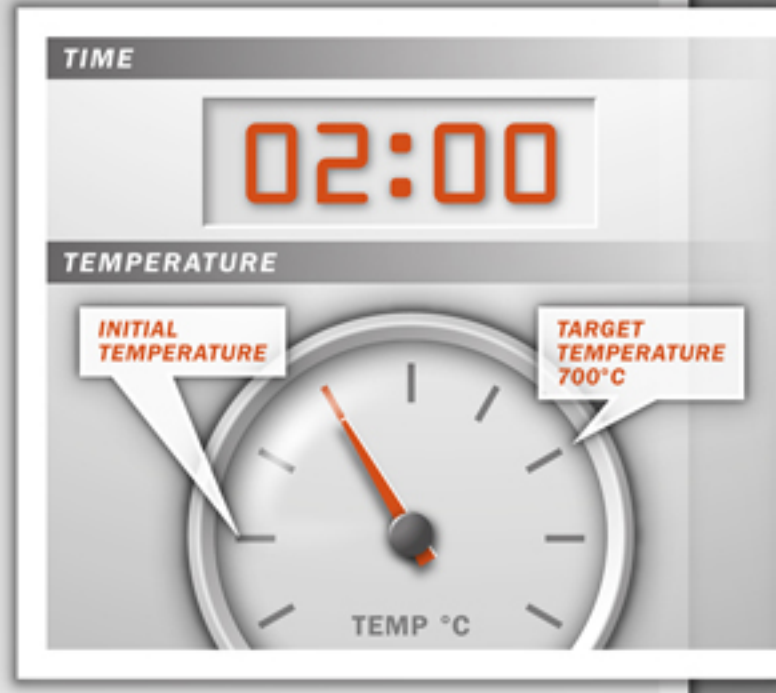




Continue the heating to raise temperature at a controlled rate through a reproducible prescribed temperature profile.

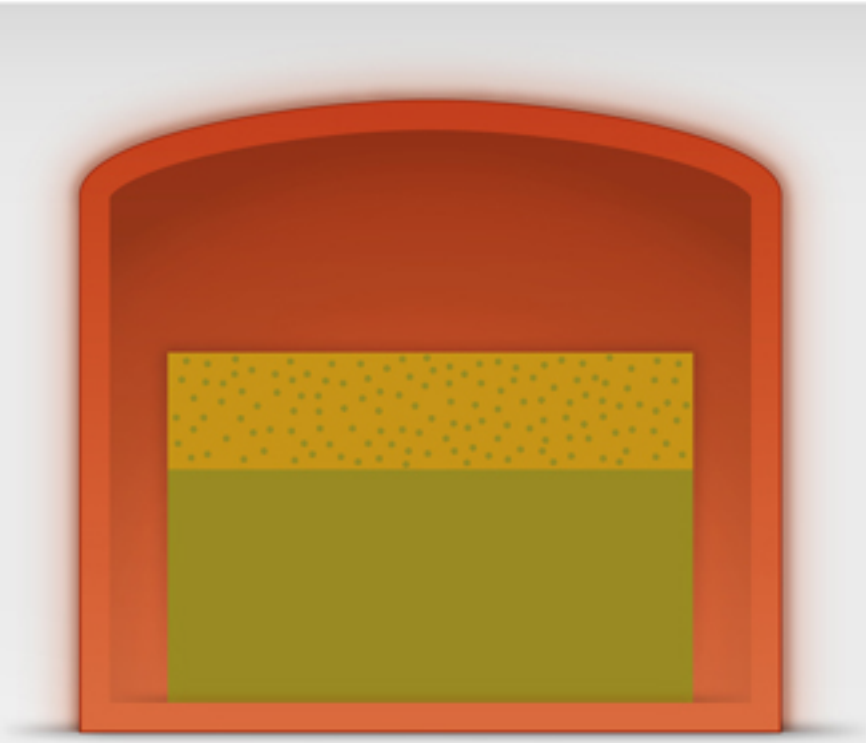
Method for Manufacturing a Polycrystalline Layer on a Substrate

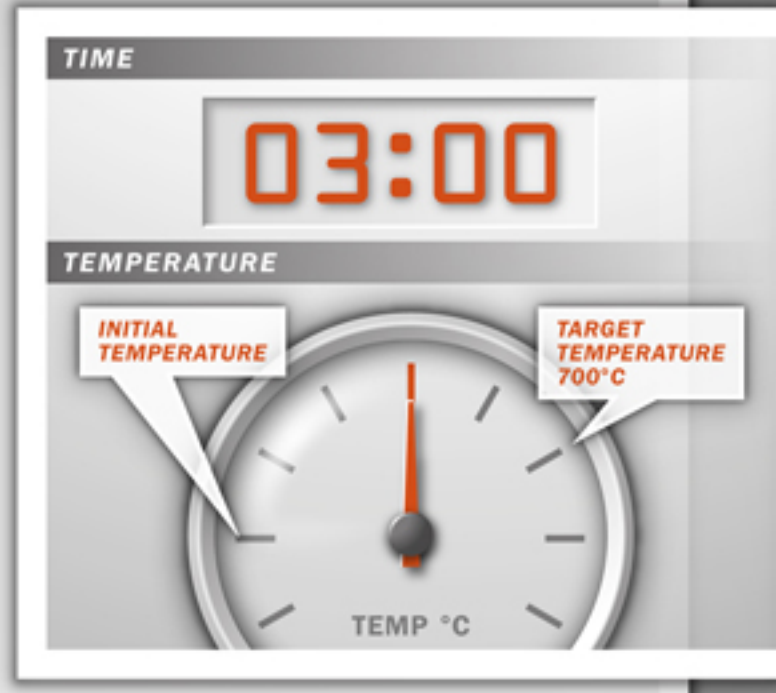




Continue the heating to raise temperature at a controlled rate through a reproducible prescribed temperature profile.

Method for Manufacturing a Polycrystalline Layer on a Substrate





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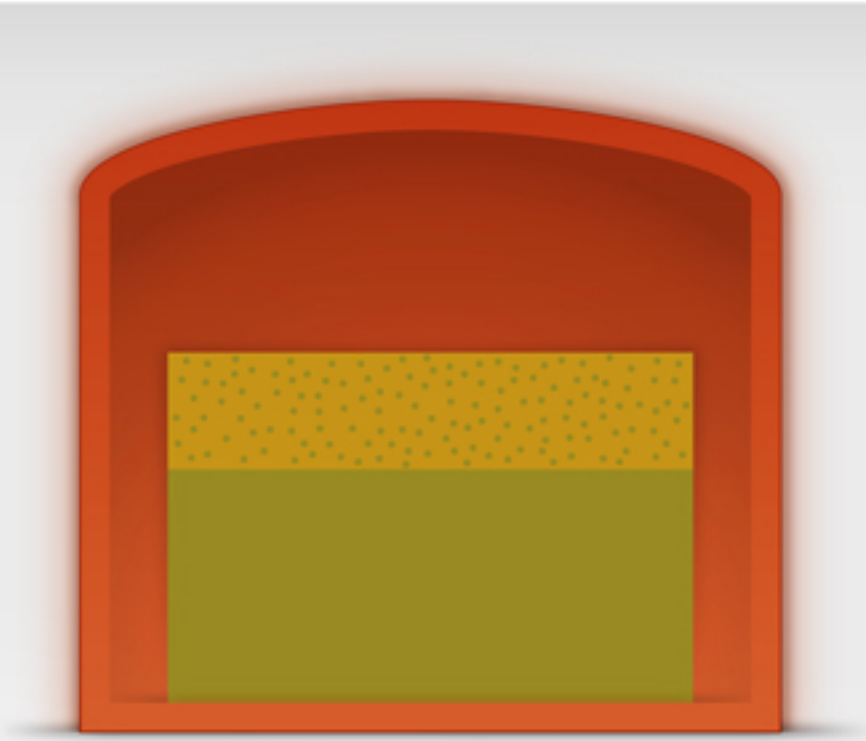
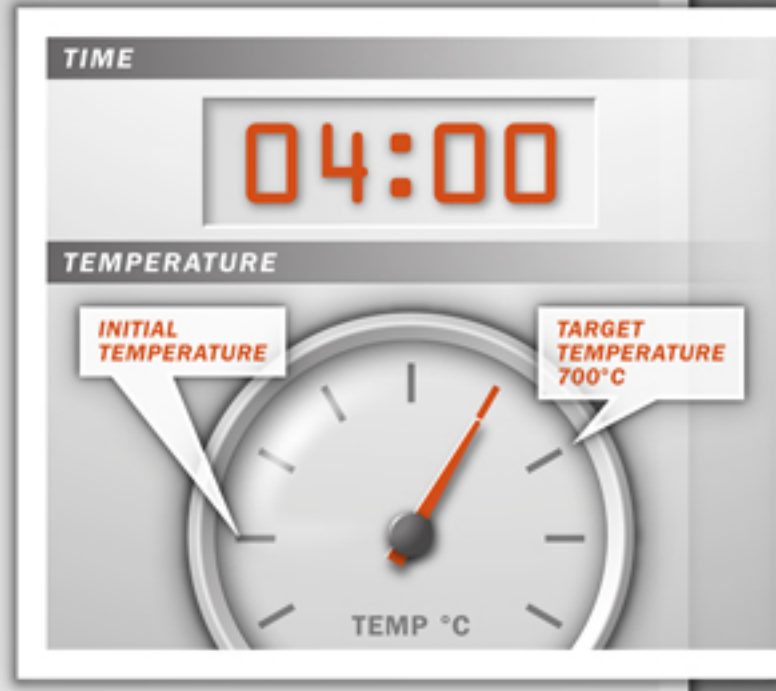
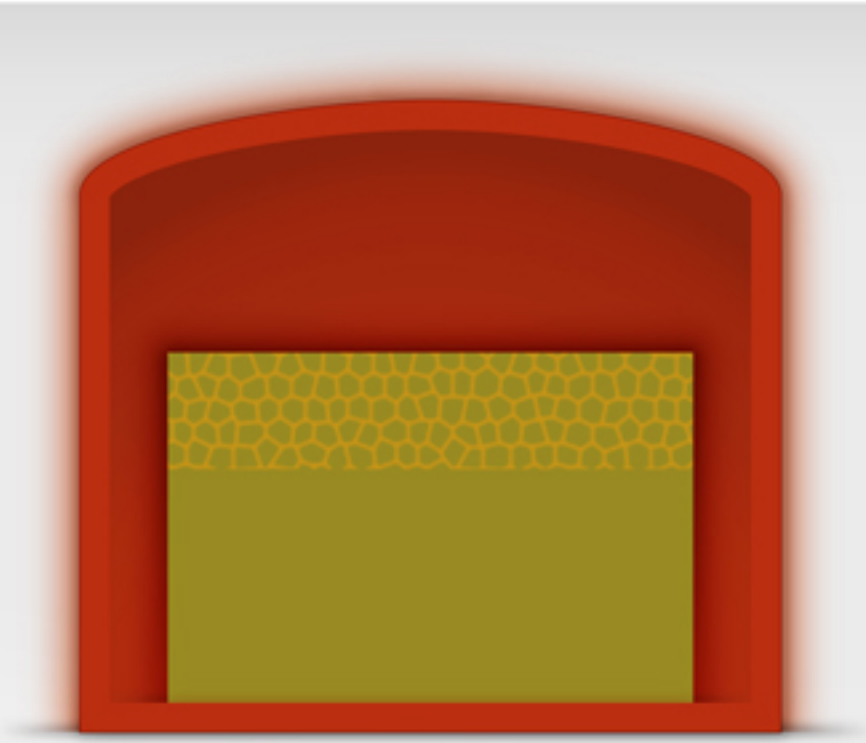
Method for Manufacturing a Polycrystalline Layer on a Substrate

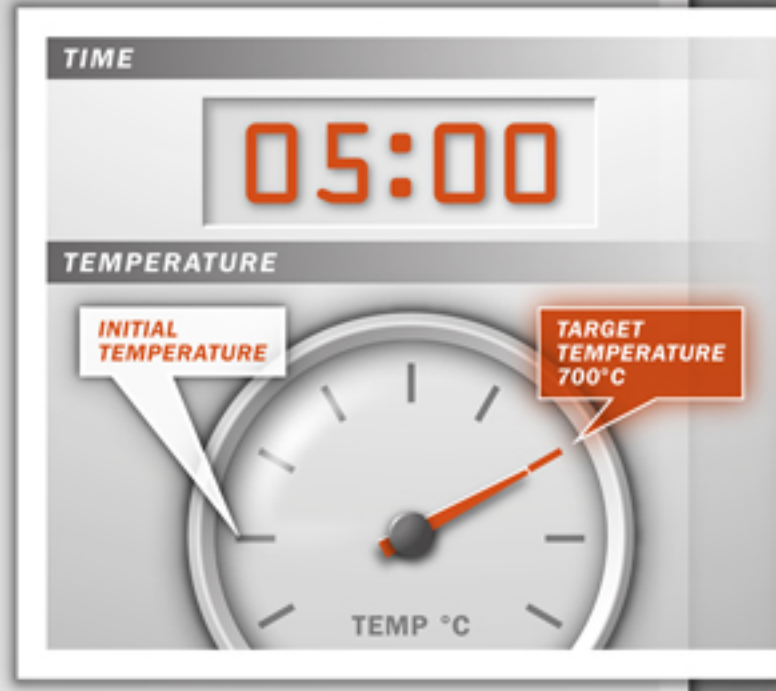




Continue the heating to raise temperature at a controlled rate through a reproducible prescribed temperature profile.

Method for Manufacturing a Polycrystalline Layer on a Substrate



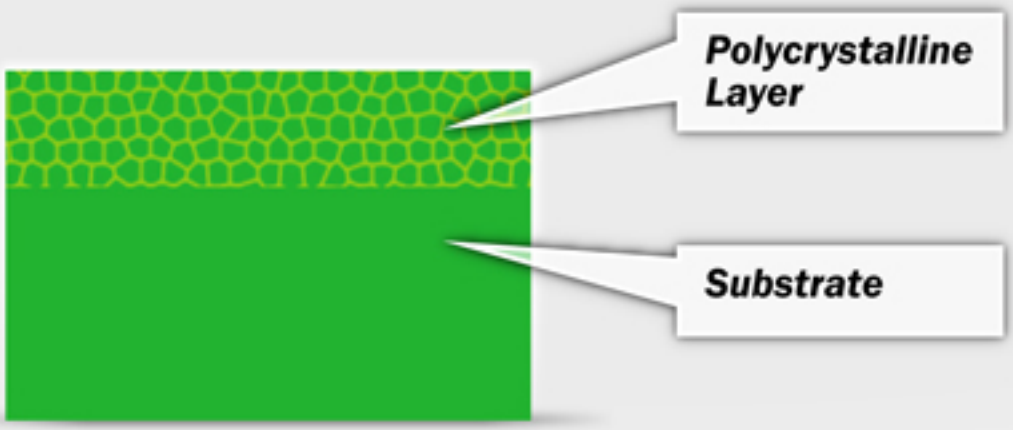


At the target temperature, the amorphous silicon layer crystallizes into the desired polycrystalline layer.

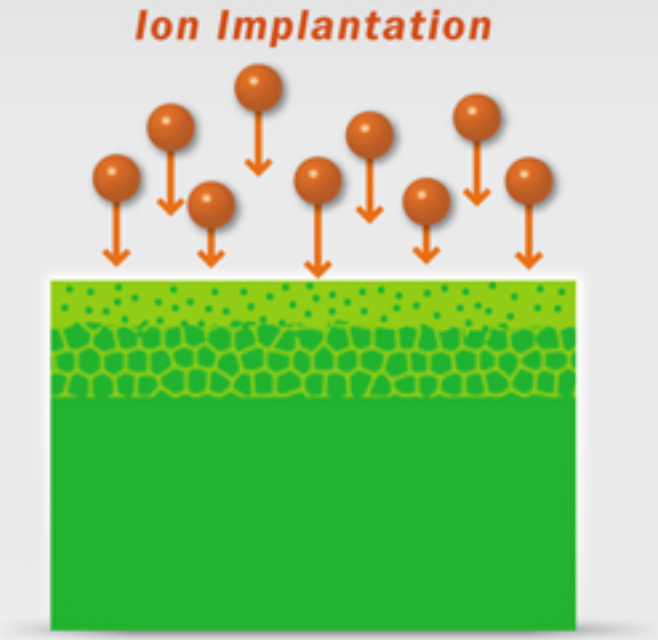
Method for Manufacturing a Polycrystalline Layer on a Substrate

The polycrystalline layer has a defined grain size and texture.

Another Method of Depositing an Amorphous Layer on Bulk Silicon Disclosed in the '670 Patent

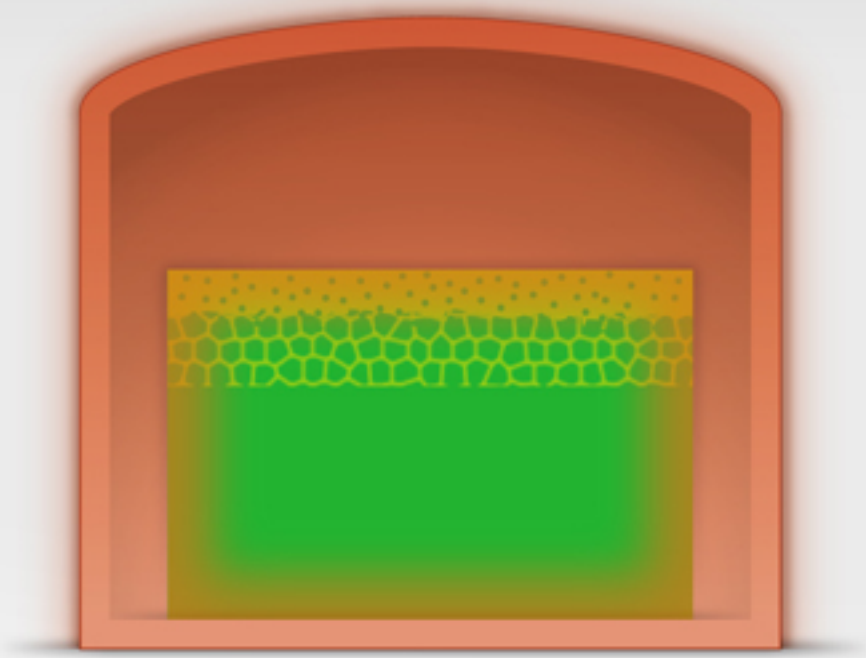


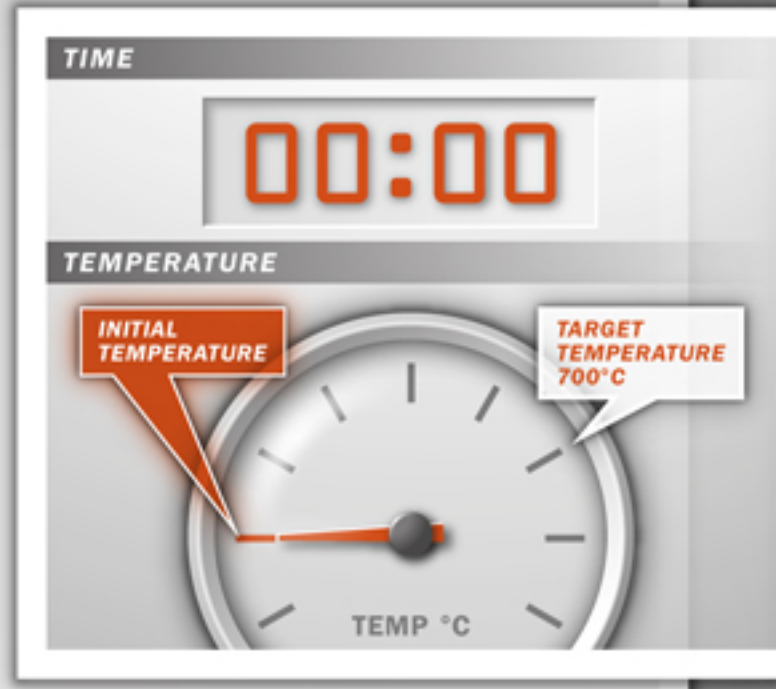
Another Method of Depositing an Amorphous Layer on Bulk Silicon Disclosed in the '670 Patent



The ion implantation step damages silicon crystal structure, causing it to become amorphous.

Another Method of Depositing an Amorphous Layer on Bulk Silicon Disclosed in the '670 Patent





Substrate with amorphous layer is heated to an initial temperature that is LOWER than the crystallization temperature.

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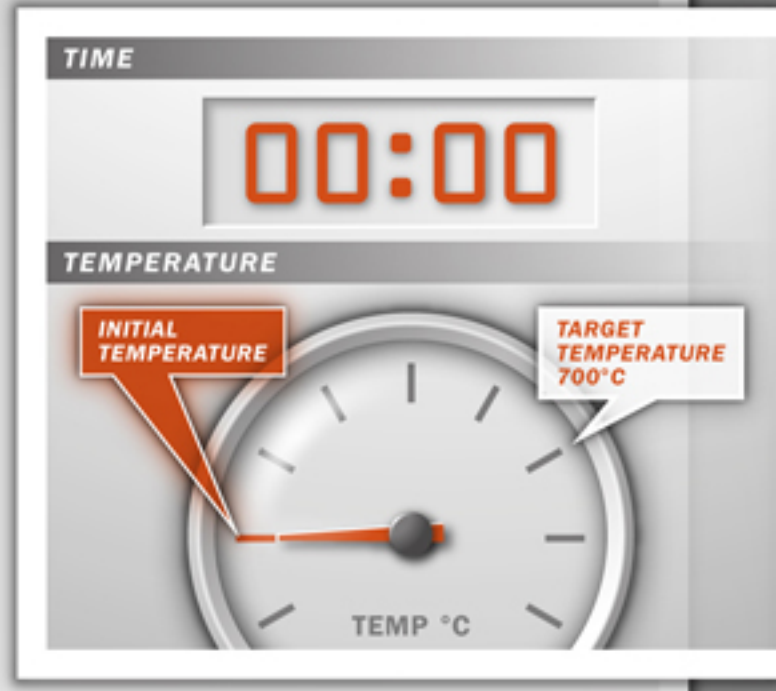

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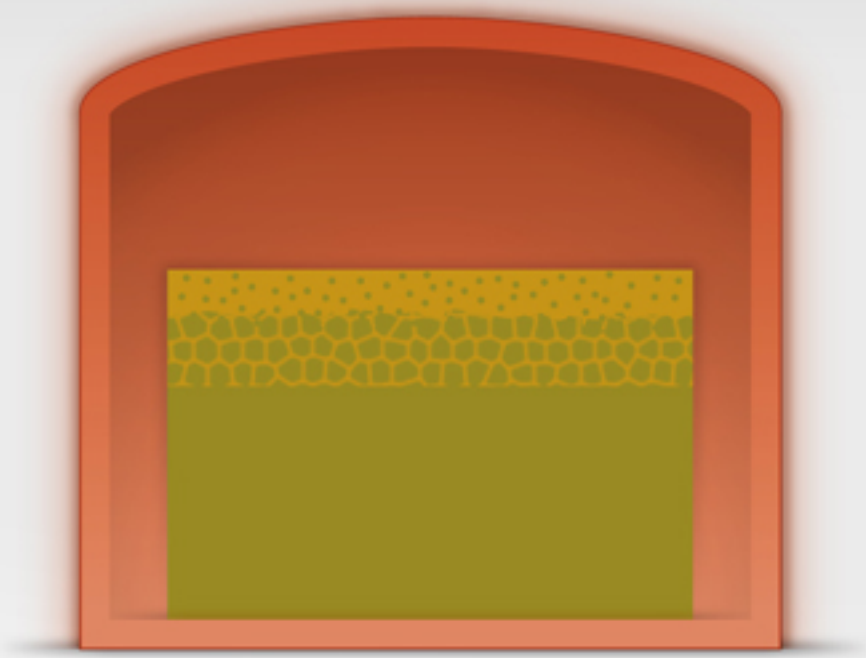

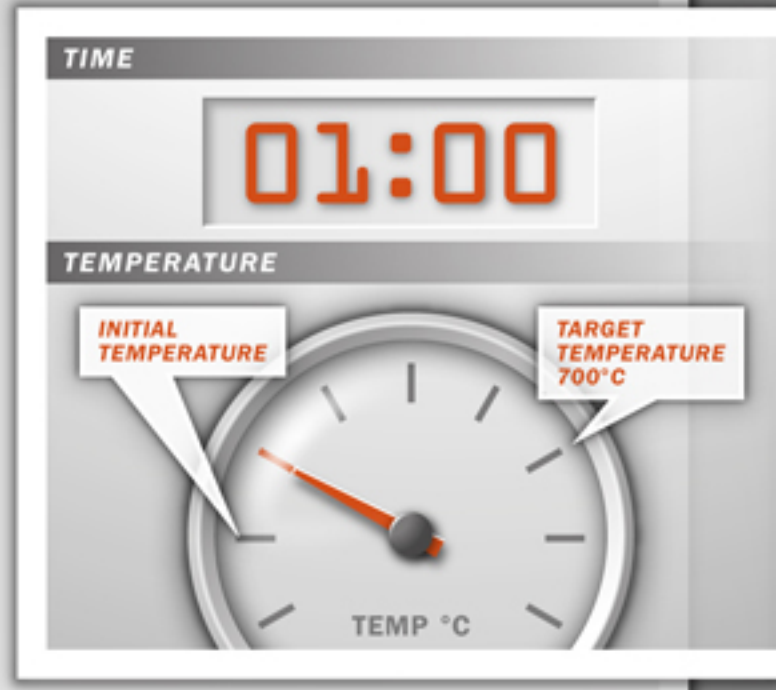

Continue the heating to raise temperature at a controlled rate through a reproducible prescribed temperature profile.

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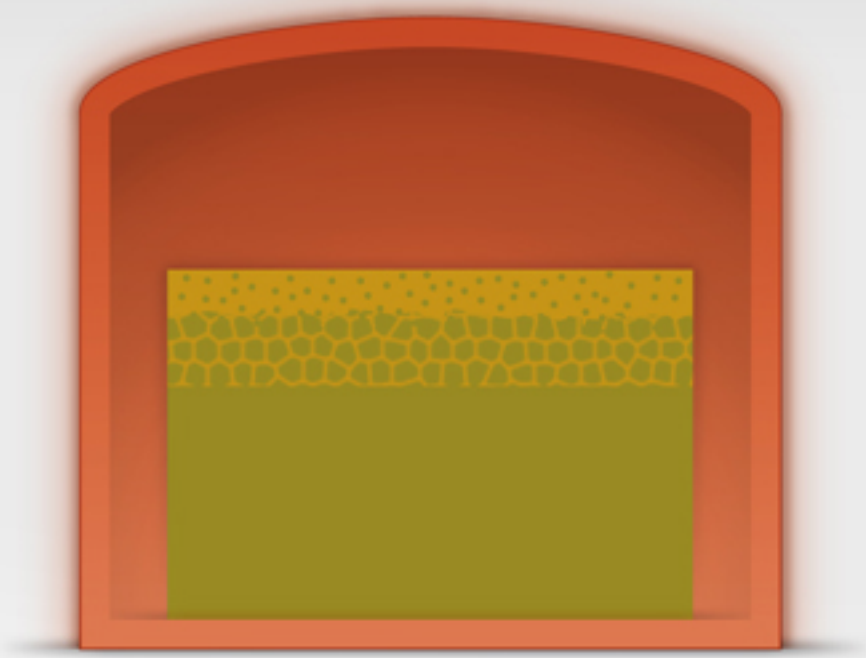

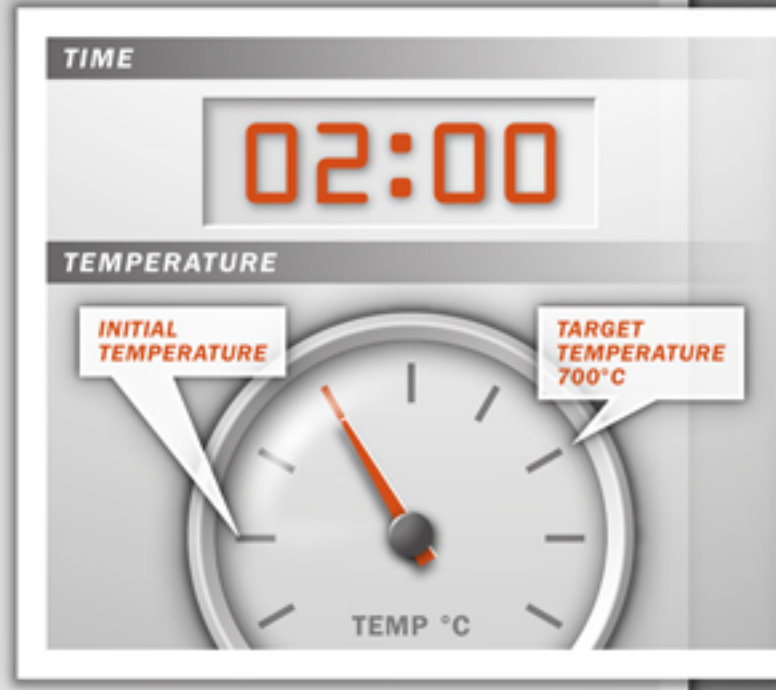

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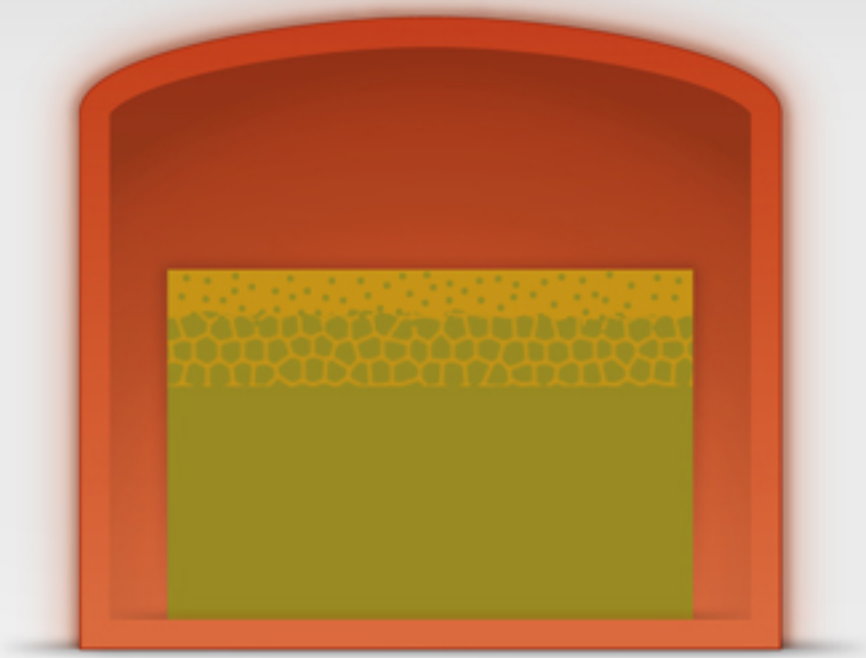

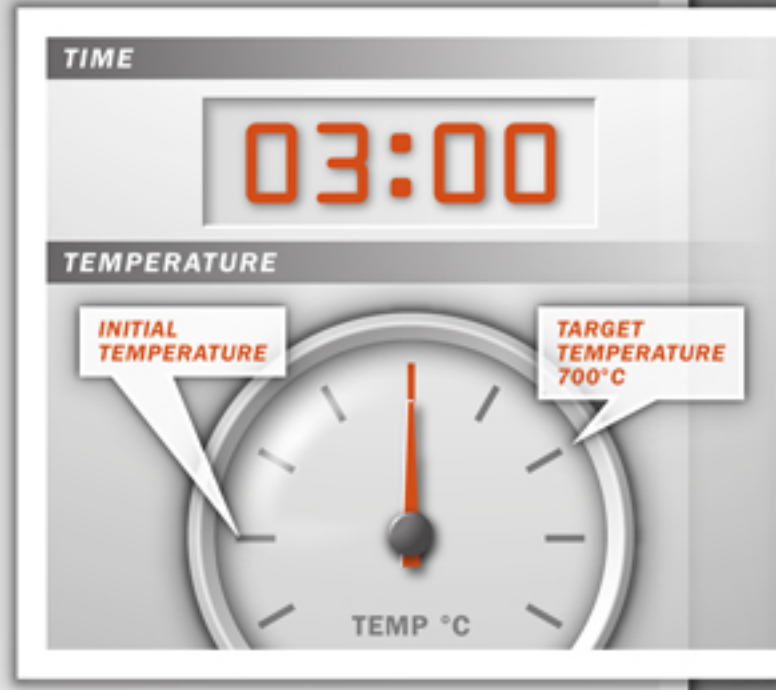

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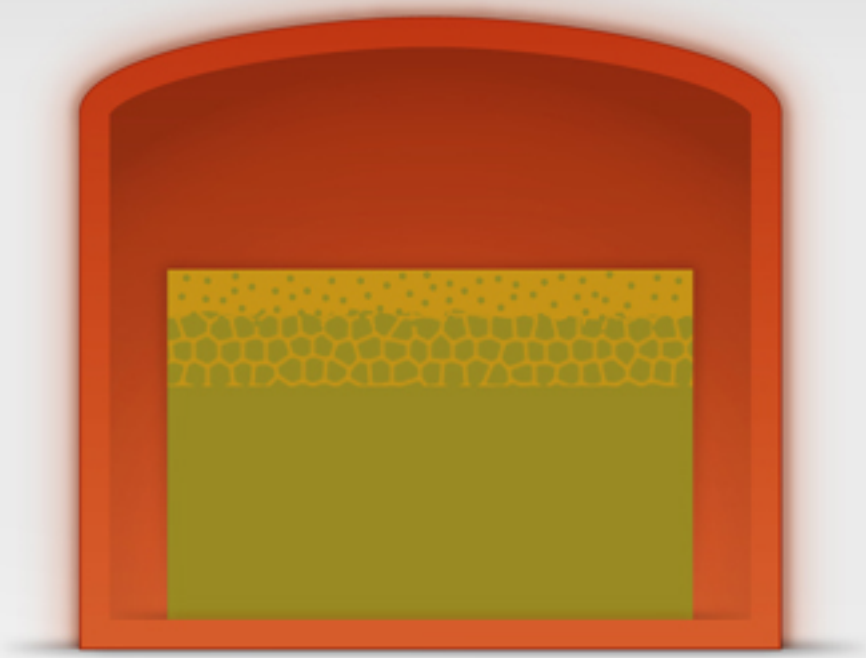

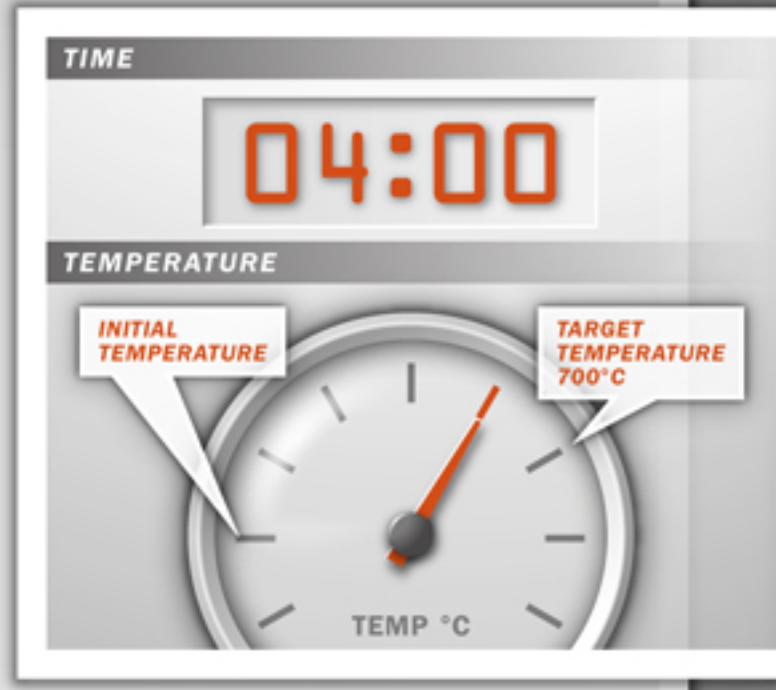

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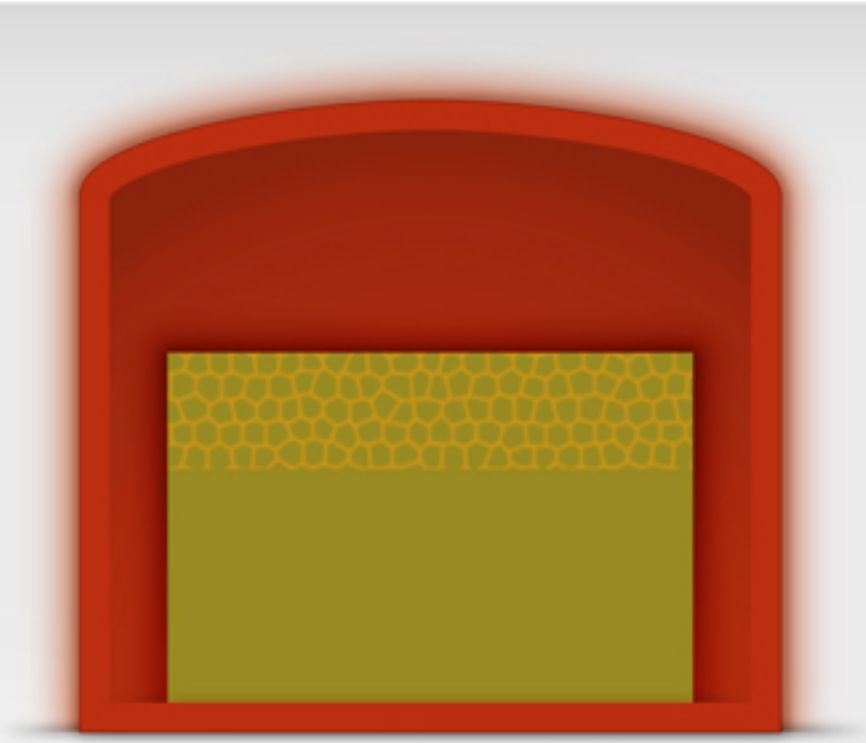

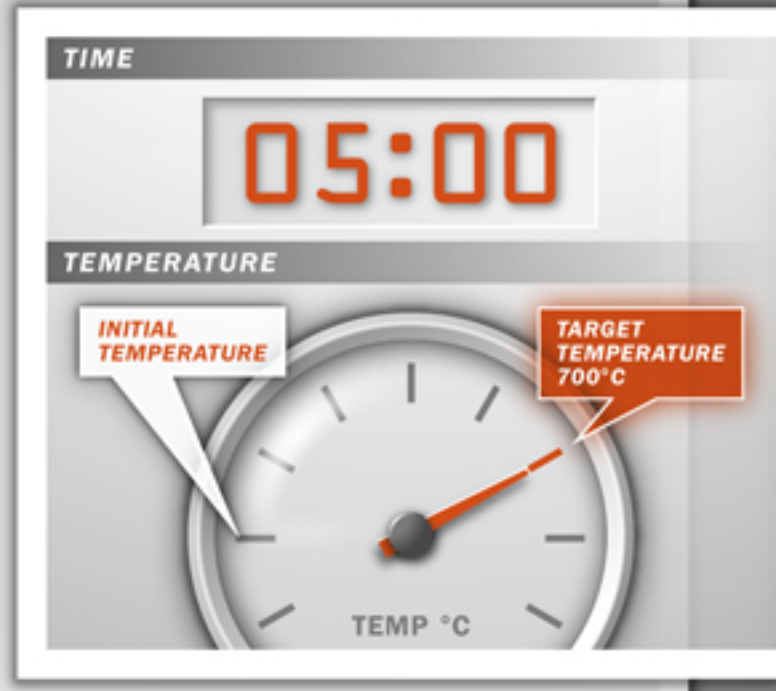

The controlled heating causes recrystallization into a polycrystalline layer having a defined grain size and texture.

Another Method of Depositing an Amorphous Layer on Bulk Silicon Disclosed in the '670 Patent

The polycrystalline layer has a defined grain size and texture.